FIXED SNOOP RESPONSE TIME FOR SOURCE-CLOCKED MULTIPROCESSOR BUSSES

ABSTRACT

An interfacing logic is implemented in one or more processors and a memory controller in a multiprocessor system. The interfacing logic enables all processors to receive snoops and snoop responses substantially at the same time by delaying data transmitted over faster busses before the data is provided to a local logic at a receiving end of the faster busses. The interfacing logic comprises two or more paths of a multiplexer component connected to a storage component. The storage components are connected to another multiplexer component for selecting one of the two or more paths. Preferably, a bus control logic in the receiving end determines how much delay is performed to compensate for delay differences between data busses.